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APPLICATION FOR U.S. LETTERS PATENT

Title:

METHOD OF FORMING A CHALCOGENIDE MATERIAL CONTAINING DEVICE

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METHOD OF FORMING A CHALCOGENIDE MATERIAL CONTAINING DEVICE

FIELD OF THE INVENTION

[0001] The invention relates to the field of random access memory (RAM) devices formed using a resistance variable material, and in particular to an improved method of manufacturing a resistance variable memory element.

BACKGROUND OF THE INVENTION

[0002] A well known semiconductor memory component is a random access memory (RAM). RAM permits repeated read and write operations on memory elements. Typically, RAM devices are volatile, in that stored data is lost once the power source is disconnected or removed. Non-limiting examples of RAM devices include dynamic random access memory (DRAM), synchronous dynamic random access memory (SDRAM), and static random access memory (SRAM). DRAMS and SDRAMS typically store data in capacitors which require periodic refreshing to maintain the stored data. Although volatile, SRAMS do not require refreshing.

[0003] Recently, resistance variable memory elements, which include programmable conductor memory elements, have been investigated for suitability as semi-volatile and non-volatile random access memory elements. Generally, a programmable conductor memory element includes an insulating dielectric material formed of a chalcogenide glass disposed between two electrodes. A conductive material, such as silver, is incorporated into the dielectric material. The resistance of the dielectric material can be changed between high resistance and low resistance states depending upon movement of the conductive material within or into and out of the dielectric material in accordance with applied voltage.

[0004] One preferred resistance variable material comprises a chalcogenide glass, for example, a Ge_xSe_{100-x} glass. One method of forming a resistance variable

memory element using chalcogenide glass includes blanket forming a lower electrode over a substrate, forming one or more layers of chalcogenide glass and one or more metal, e.g., silver, containing layers over the lower electrode, and forming an upper electrode over the stack of layers. Photolithographic and etching processes are conducted to form etched stacks, each forming a resistance variable memory element. Current methods that employ these processes present various drawbacks.

[0005] Typical etch chemistries produce inherent sidewalls of chemical compounds on the stack of layers. The wet scrub used to remove the etch sidewalls has been known to scratch the stack surface or remove the top layer of the stack entirely, decreasing device functionality. Problems are also encountered in removing the photoresist used to pattern the structures. Such problems include residual organic material and material loss from the stack. Stack material is lost because photo developers containing Tetramethylammonium Hydroxide (TMAH) etch away the stack material. Typically, when structures or devices do not conform to desired specifications, a rework is performed to make the nonconforming structures/devices conform to the desired specifications. Photolithographic rework is a form of rework that includes photolithographic processes. Due to the material loss, however, photolithographic rework is not always possible.

[0006] Further, dry etching has not been a suitable process. Exposure to dry etch or dry strip plasmas are known to cause silver to migrate out of the stack, which can result in a "racetrack" defect. FIG. 1 illustrates a memory array 10, which has the "racetrack" defect. The memory elements in the periphery or "racetrack" portion 14 of the array 10 are affected by silver migration during the dry etch, whereas the center memory elements 12 are unaffected. It is believed that the silver migration is caused by light exposure during the etch process. It is desirable to eliminate the racetrack defect.

[0007] It is desirable to have an improved method of fabricating a resistance variable memory element, which addresses one or more of the above disadvantages of conventional photolithographic and etching processes.

BRIEF SUMMARY OF THE INVENTION

[0008] Embodiments of the invention provide a method of forming a chalcogenide material containing device, and particularly resistance variable memory elements. A stack of one or more layers is formed over a substrate. The stack includes a layer of chalcogenide material and a metal, e.g., silver, containing layer. A protective layer is formed over the stack. The protective layer blocks light, is conductive, and is etchable with the other layers of the stack. Further, the metal of the metal containing layer is substantially insoluble in the protective layer. The stack and the protective layer are then patterned and etched to form memory elements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of exemplary embodiments provided below with reference to the accompanying drawings in which:

[0010] FIG. 1 illustrates a conventional memory array;

[0011] FIG. 2 illustrates cross-sectional views of a memory element fabricated in accordance with an exemplary embodiment of the invention and at an initial stage of processing;

[0012] FIGS. 3-8 illustrate cross-sectional views of the memory element of FIG. 2 at intermediate stages of processing;

[0013] FIG. 9 illustrates a cross-sectional view of a memory element in accordance with another exemplary embodiment of the invention;

[0014] FIG. 10 illustrates a cross-sectional view of the memory element of FIG. 9 at an initial stage of processing;

[0015] FIG. 11 illustrates a memory array having a memory element in accordance with the invention; and

[0016] FIG. 12 illustrates a computer system including the memory array of FIG. 11.

DETAILED DESCRIPTION OF THE INVENTION

[0017] In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed, and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

[0018] The term "substrate" used in the following description may include any supporting structure including, but not limited to, a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a semiconductor substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation. The substrate need not be semiconductor-based, but can be any support structure suitable for supporting an integrated circuit. For example, the substrate can be ceramic or polymer-based.

[0019] The term "silver" is intended to include not only elemental silver, but silver with other trace metals or in various alloyed combinations with other metals as known in the semiconductor industry, as long as such silver alloy is conductive, and as long as the physical and electrical properties of the silver remain unchanged.

[0020] The term "silver-selenide" is intended to include various species of silver-selenide, including some species which have a slight excess or deficit of silver, for instance, Ag_2Se, $Ag_{2+x}Se$, and $Ag_{2-x}Se$.

[0021] The term "resistance variable memory element" is intended to include any memory element, including Programmable Conductive Random Access Memory (PCRAM) elements, which exhibit a resistance change in response to an applied voltage.

[0022] The term "chalcogenide glass" is intended to include glasses that comprise an element from group VIA (or group 16) of the periodic table. Group VIA elements, also referred to as chalcogens, include sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O).

[0023] Embodiments of the invention provide a method of forming a chalcogenide material containing device, such as, and without limitation, a resistance variable memory element, that does not suffer from the drawbacks associated with conventional fabrication methods. One or more layers including a layer of chalcogenide material and a metal containing layer are formed over a substrate. The chalcogenide material layer and the metal containing layer can be a same layer. A protective layer is formed over the layer(s). The protective layer blocks light, is conductive, and is etchable with the other layers of the stack. Further, the metal of the metal containing layer is substantially insoluble in the protective layer. The chalcogenide material and metal containing layer(s) and the protective layer can be patterned and etched using conventional photolithographic and etching techniques without the above described disadvantages. Accordingly, photolithographic rework can be more readily performed on resulting structures.

[0024] Specific exemplary embodiments of the invention are now explained with reference to the figures, where like reference numbers indicate like features. Although the exemplary embodiments described herein refer to the formation of only one resistance variable memory element 200, it must be

understood that the invention contemplates the formation of any number of such resistance variable memory elements, which can be fabricated in a memory array and operated with memory element access circuits.

[0025] FIGS. 2-8 show an exemplary processing sequence for forming a resistance variable memory element 200 according to an exemplary embodiment of the invention. Referring to FIG. 2, a via 203 is etched in a substrate 201 by any suitable techniques. A first electrode 202 is formed in the via 203, as illustrated in FIG. 3. The first electrode 202 may comprise any conductive material, for example, tungsten, nickel, tantalum, aluminum, platinum, conductive nitrides, and other materials. The first conductive layer is planarized to the surface of the substrate 201.

[0026] A stack 420 of layers 421, 422, 423, 424, 425 is sequentially formed over the substrate 201 and the first electrode 202, as shown in FIG. 4. The stack 420 of layers 421, 422, 423, 424, 425 is exemplary and it should be understood that the memory element 200 can have a different layer structure and can include additional or fewer layers than those illustrated.

[0027] Layer 421 is a first chalcogenide glass layer, and can be germanium-selenide glass having a Ge_xSe_{100-x} stoichiometry. It is desired that the stoichiometric range is between approximately $Ge_{20}Se_{80}$ to approximately $Ge_{43}Se_{57}$ and preferably approximately $Ge_{40}Se_{60}$. The first chalcogenide glass layer 421 can have a thickness of approximately 100 Å to approximately 1000 Å and is preferably approximately 150 Å.

[0028] The formation of the first chalcogenide glass layer 421 can be accomplished by any suitable method. For instance, germanium-selenide glass can be formed by evaporation, co-sputtering germanium and selenium in the appropriate ratios, sputtering using a germanium-selenide target having the desired stoichiometry, or chemical vapor deposition with stoichiometric amounts of GeH_4 and SeH_2 gases (or various compositions of these gases), which result in a germanium-selenide film of the desired stoichiometry.

[0029] Layer 422 is a metal containing layer and can be directly deposited on the surface of the first chalcogenide glass layer 421. When the metal containing layer 422 is a silver-selenide layer rather than a metal layer, such as a silver layer, doping the chalcogenide glass layer 421 by photodoping or thermal diffusion is unnecessary to induce silver migration into the chalcogenide glass layer 421. However, doping the chalcogenide glass layer 421 with a metal (e.g., silver) is an optional variant.

[0030] The metal containing layer 422 can be any suitable metal containing layer which can supply metal into the chalcogenide glass layer 421. Suitable metal containing layers include silver-chalcogenide layers, such as silver-sulfide, silver-oxide, silver-telluride, and silver-selenide. A variety of processes can be used to form the metal containing layer 422, which is preferably silver-selenide. For instance, physical vapor deposition techniques such as evaporative deposition and sputtering may be used. Other processes such as chemical vapor deposition, co-evaporation, or deposition of a layer of selenium above a layer of silver to form a silver-selenide layer can also be used.

[0031] It is desired that the thickness of the metal containing layer 422 is such that a ratio of the metal containing layer 422 thickness to the first chalcogenide glass layer 421 thicknesses is between approximately 5:1 and approximately 1:1. In other words, the thickness of the metal containing layer 422 is between approximately 1 to approximately 5 times greater than the thickness of the first chalcogenide glass layer 421. Preferably, the ratio is between approximately 3.1:1 and approximately 2:1. In the exemplary embodiment of FIG. 4, layer 421 is approximately 150 Angstroms (Å) thick and layer 422 is approximately 470 Å thick (i.e., ratio of 3.1:1).

[0032] A second glass layer 423 is formed over the first metal containing layer 422. When the metal containing layer is silver-selenide, the second glass layer

423 allows deposition of silver above the silver-selenide layer, while preventing agglomeration of silver on the surface of the silver-selenide.

[0033] The second glass layer 423 may also act as a silver diffusion control layer or an adhesion layer. For use as a diffusion control layer, any suitable glass may be used, including but not limited to chalcogenide glasses. Illustratively, the second chalcogenide glass layer 423 has the same stoichiometric composition as the first chalcogenide glass layer, e.g., Ge_xSe_{100-x}. The second glass layer 423, however, can be of a different material, have a different stoichiometry, and/or be more rigid than the first chalcogenide glass layer 421. When used as a diffusion control layer, the second glass layer 423 can comprise SiSe (silicon-selenide), AsSe (arsenic-selenide, such as As_3Se_2), GeS (germanium-sulfide), and combinations of Ge, Ag, and Se. Any one of these suitable glass materials can further comprise small concentrations, e.g., less than approximately 3%, of dopants to include nitrides, metal, and other group 13-16 elements from the periodic table.

[0034] The thickness of the layers 422, 423 are such that the metal containing layer 422 thickness is greater than the thickness of the second glass layer 423. It is desired that a ratio of the metal containing layer 422 thickness to the second glass layer 423 thickness is between approximately 5:1 and approximately 1:1. Preferably, the ratio of the metal containing layer 422 thickness the second glass layer 423 thickness is between approximately 3.3:1 and approximately 2:1. The second glass layer 423 preferably has a thickness between approximately 100 Å to approximately 1000 Å. In the exemplary embodiment of FIG. 4, layer 423 has a thickness of approximately 150 Å. The second glass layer 423 can be formed by any suitable method. For example, by chemical vapor deposition, evaporation, co-sputtering, or sputtering using a target having the desired stoichiometry.

[0035] A silver layer 424 is formed above the second chalcogenide glass layer 423. The silver layer 424 may be deposited over the second glass layer 423 by any suitable means, such as sputtering or plating techniques, including electroplating

or electroless plating. In the illustrated embodiment, the thickness of the silver layer 424 is illustratively approximately 200 Å.

[0036] A conductive adhesion layer 425 is formed over the silver layer 424. Suitable materials for the conductive adhesion layer 425 include conductive materials capable of providing good adhesion between the silver layer 424 and a protective layer 529 (FIG. 5). Desirable materials for the conductive adhesion layer 425 include chalcogenide glasses. The conductive adhesion layer 425 may be the same chalcogenide glass material used in the first and second chalcogenide glass layers 421, 423 discussed above. The thickness of the chalcogenide glass conductive adhesion layer 425 is illustratively approximately 100 Å.

[0037] In the exemplary embodiment of FIG. 4, during the formation and processing of the memory element 200, silver diffuses into layers 423 and 425. This results in layers 423-425 comprising $Ge_xSe_{100-x}Ag_y$. For simplicity purposes only, however, these layers are shown individually in each of FIGS. 4-10.

[0038] Referring to FIG. 5, the protective layer 529 is formed over the conductive adhesion layer 425 to a thickness between approximately 50 Å and approximately 500 Å. The protective layer 529 comprises a conductive material in which the metal, e.g., silver, of metal containing layer 422 is not soluble. It should be noted, however, that processes used to form protective layer 529 (e.g., sputtering) can result in silver in the protective layer 529. The protective layer 529 also blocks light and is etchable. Illustratively, protective layer 529 is a layer of tungsten. Alternatively, protective layer 529 can be a composite tungsten/tantalum nitride layer. The protective layer 529 can be formed by any suitable techniques.

[0039] The protective layer 529 and stack 420 are patterned and etched using standard photolithographic and etching techniques to form a pillar structure, as shown in FIG. 6. A photoresist layer 660 is formed over the protective layer 529. Portions of the photoresist layer 660 are exposed to light and developed to remove the exposed portions (not shown) and form a desired pattern of photoresist on the

protective layer 529. For this process, a photo developer containing TMAH can be used.

[0040] The protective layer 529 and stack 420 are then etched. Suitable etching techniques can include a halogen containing reactive ion etch (RIE) process or an argon (Ar) sputter etch process. For example, when the protective layer 529 is greater than approximately 100 Å, the protective layer 529 can be etched using a halogen containing RIE process, and the stack 420 can be etched using an Ar sputter etch process. When the metal layer thickness is less than approximately 100 Å, the protective layer 529 and the stack 420 can be etched using an Ar sputter etch process.

[0041] As shown in FIG. 6, the etching process results in sidewalls 661 on the sides of the stack 420. After the protective layer 529 and the stack 420 are etched, the photoresist 660 and sidewalls 661 are removed, for example, by using a wet acid process or a dry strip process, as shown in FIG. 7. To remove the photoresist 660 and sidewalls 661, a scrub step can also be conducted.

[0042] The protective layer 529 protects the layers 421-425 from scrubber damage during photoresist 660 and sidewall 661 removal. Additionally, because photoresist 660 does not directly contact layer 425, it can be more easily removed. For example, photoresist 660 does not adhere well to tungsten, and where the protective layer 529 is tungsten, the photoresist 660 is easily removed. Further, the protective layer 529 protects the layers 421-425 from the TMAH containing photo developer. This results in less material loss and enables photolithographic rework. The protective layer 529 also decreases dry etch induced defects in the stack 420 by decreasing the exposure of the layers 421-425 to the plasma. Further, because the protective layer 529 blocks light, the racetrack defect (FIG. 1) is avoided. Therefore, the method according to the invention does not suffer from the drawbacks associated with conventional fabrication methods.

[0043] Referring to FIG. 8, a second (top) electrode 880 is formed over the stack 420 and protective layer 529. Since the metal, e.g., silver, of metal containing layer 422 is not soluble in the protective layer 529, the protective layer 529 serves to keep silver out of the electrode 880. Illustratively, the second electrode 880 is a common electrode and can be shared among a plurality of memory elements (not shown). The second electrode 880 can be any conductive material, such as tungsten, nickel, tantalum, aluminum, platinum, silver, conductive nitrides, and others. The second electrode 880 is preferably tungsten or tantalum nitride.

[0044] In an alternative exemplary embodiment, the memory element 200 can include a common first (bottom) electrode 902, instead of a common second electrode, as shown in FIG. 9. In such a case, an optional insulating layer (not shown) can be formed over the substrate 201. The optional insulating layer can be formed by any known deposition methods, such as sputtering by chemical vapor deposition (CVD), plasma enhanced CVD (PECVD) or physical vapor deposition (PVD). The optional insulating layer can be formed of a conventional insulating oxide, such as silicon oxide (SiO_2), a silicon nitride (Si_3N_4), or a low dielectric constant material, among many others.

[0045] A first electrode 902 is formed over the substrate 201, as shown in FIG. 10. The first electrode 902 may comprise any conductive material, for example, tungsten, nickel, tantalum, aluminum, platinum, conductive nitrides, and other materials. A dielectric layer 903 is formed over the first electrode 902. The dielectric layer 903 can comprise the same or different materials as those described above for the optional insulating layer.

[0046] An opening (not shown) extending to the first electrode 902 is formed in the first dielectric layer 903. The opening can be formed by known methods in the art, for example, by a conventional patterning and etching process. A stack 420 comprising layers 421, 422, 423, 424, and 425 is formed over the first

electrode 902 as described above in connection with FIGS. 4-8. Instead, however, of a protective layer 529, a second electrode 990 is formed over the stack 420. The second electrode 990 is formed of the same material as is suitable for protective layer 529. Accordingly, the second electrode 990 comprises a conductive material which blocks light, is etchable, and is a material in which the metal of layer 422, e.g., silver, is not soluble. By forming the second electrode 990 of such a material, the benefits described above in connection with FIGS. 6 and 7 can be realized. Illustratively, second electrode 990 is tungsten. Alternatively, second electrode 990 can be a composite layer of tungsten and tantalum nitride.

[0047] The stack 420 and second electrode 990 can be patterned and etched as described above in connection with FIGS. 6-7 to form a memory element 200 having the structure shown in FIG. 9.

[0048] Referring to FIG. 11, a memory element 200 in accordance with the invention can be included in a memory array 1100. In turn, the memory array 1100 can be included in a memory device 1248 and used in a processor based system 1200, depicted in FIG. 12.

[0049] FIG. 12 is a block diagram of a processor-based system 1200 which includes a memory circuit 1248, for example a programmable conductor RAM employing resistance variable memory elements 200 fabricated in accordance with the invention. The processor system 1200, such as a computer system, generally comprises a central processing unit (CPU) 1244, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 1246 over a bus 1252. The memory 1248 communicates with the system over bus 1252 typically through a memory controller.

[0050] In the case of a computer system, the processor system may include peripheral devices such as a floppy disk drive 1254 and a compact disc (CD) ROM drive 1256, which also communicate with CPU 1244 over the bus 1252. Memory

1248 is preferably constructed as an integrated circuit, which includes one or more resistance variable memory elements 200. If desired, the memory 1248 may be combined with the processor, for example CPU 1244, in a single integrated circuit.

[0051] The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modification and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.